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Code No: 153AT

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February - 2024

ELECTRONIC DEVICES AND CIRCUITS

(Common to ECE, EIE, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Differentiate Transition Capacitance and Diffusion Capacitance.	[2]
b)	In a clamping circuit R_r =200kΩ, and R_f=300Ω, find resultant resistance value.	[3]
c)	Define Early Effect.	[2]
d)	Why BJT is called as Current Controlled Device?	[3]
e)	Define Amplification factor in JFET.	[2]
f)	Draw the equivalent circuit for tunnel diode.	[3]
g)	Name factors influencing the low-frequency cutoff in BJT amplifiers.	[2]
h)	What are the advantages of h-parameter analysis?	[3]
i)	Why the input impedance of FET is higher than BJT?	[2]
j)	Define the threshold voltage $V_{gs(th)}$ in MOSFET and its significance.	[3]

PART – B

(50 Marks)

2.a) Illustrate about the switching characteristics of PN junction diode with suitable diagrams.

b) Consider a silicon PN junction at T = 300 K, with doping concentrations of Na = 1016cm^{-3} and Nd = 1015cm^{-3}. Assume that n_i = 1.5 × 1010 cm^{-3}. Let C_{j0} = 0.5pF. Calculate the junction capacitance at V_R=1V and V_R = 5V. [5+5]

OR

3.a) Explain the working of a Full wave Bridge Rectifier and derive its average voltage, RMS voltage, Peak factor, Form factor, Form factor and Rectification efficiency.

b) A symmetrical 50 Hz square wave whose peak to peak excursions are ± 100 V with respect to ground is to be negatively clamped at 25 V. Draw the necessary circuit diagram and output waveform for this purpose. [6+4]

4.a) With neat diagram, explain the input and output characteristics of a transistor in CE configuration.

b) A transistor is operated at a forward current of 2μA and with the collector open circuited. Calculate the junction voltages V_C and V_E, the collector to emitter voltage V_{CE} assuming I_{CO} = 2μA, I_{EO} = 1.6μA and α_N = 0.98. [6+4]

OR

5.a) Determine the quiescent currents and the collector to emitter voltage for a Ge transistor with $\beta = 50$ in the self biasing arrangements. The circuit component values are $V_{CC} = 20V$, $R_C = 2k\Omega$, $R_e = 0.1\ k\Omega$, $R_1 = 100\ k\Omega$ and $R_2 = 5\ k\Omega$. Find the stability factor S.

b) Explain the need for biasing in electronic circuits. What are the factors affecting the stability factor? Explain. [5+5]

6.a) Describe the construction and operation of P-channel JFET with neat diagrams.

b) Analyze how zener diode is used in Voltage regulation with a neat circuits. [5+5]

OR

7.a) Illustrate the working of Varactor Diode using Energy Band Diagrams.

b) Explain, how FET is working as Voltage Variable Resistor. [5+5]

8.a) For a common collector circuit draw the h-parameter equivalent circuit and write the expressions for input impedance and output impedance.

b) The h parameters for the transistor are h_{ie} =1.1kΩ, h_{fe} = 99, h_{re} = 2.5×10^{-4} and h_{oe} = 25μA/V. Find the h parameters for common base and common collector configurations. [5+5]

OR

9.a) Draw and explain the low-frequency response of BJT amplifiers.

b) A common emitter (CE) amplifier has emitter resistance (R_e) 500 ohms, capacitance in parallel with R_e (Ce) is 10 μF, load resistance (R_L) is 1 kohm, Input capacitance (C_{in}) is 5 μF, transition frequency (f_t) is 50 MHz. Calculate the low-frequency cutoff (f_L) and high-frequency cutoff (f_H) of the amplifier. Determine the bandwidth. [5+5]

10.a) Describe the operation of common drain FET amplifier and derive the equation for voltage gain.

b) A JFET amplifier in common gate (CG) configuration has $g_m = 4mS$ and $r_s = 200\Omega$. If the input voltage $V_{in} = 50mV$, calculate the small signal output voltage(V_{out}). [5+5]

OR

11.a) Explain the JFET Small signal Model.

b) For a P-channel MOSFET operating in depletion mode, given $V_{gs(th)} = -3V$ and $K_p = 0.8mA/V^2$, calculate the drain current(I_D) when $V_{gs} = -1V$ and $V_{ds} = 4V$. [5+5]

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